WHAT IS CLAIMED IS:

1. A capacitor, comprising:

a substrate;

a first electrically conductive layer fixed to the substrate;

a release layer fixed to a portion of the electrically conductive layer; and

a second electrically conductive layer comprising an anchor portion and a free portion, the anchor portion being fixed to the release layer, wherein the free portion is initially fixed to the release layer, but is released from the release layer to become separated from the release layer, and wherein an inherent stress profile in the second electrically conductive layer biases the free portion away from the release layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and the second electrically conductive layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer, thereby increasing the capacitance of the capacitor.

2. The capacitor of claim 1, wherein the release layer comprises an electrically insulating material.

3. The capacitor of claim 1, further comprising a dielectric layer between the release layer and the first electrically conductive layer, wherein the dielectric layer extends substantially between the free portion and the first electrically conductive layer.

4. The capacitor of claim 1, wherein the free portion is biased away from the first electrically conductive layer along a radius of curvature.

5. The capacitor of claim 4, wherein a tip of the first portion of the first electrically conductive layer is tapered.

6. A capacitor, comprising:

a substrate;

a first electrically conductive layer fixed to the substrate;

a dielectric layer fixed to a portion of the electrically conductive layer; and

a plurality of second electrically conductive layers, each second electrically conductive layer comprising an anchor portion and a free portion, the anchor portion being fixed to the dielectric layer, wherein the free portion is initially fixed to the dielectric layer, but is released from the dielectric layer to become separated from the dielectric layer, and wherein an inherent stress profile in the second electrically conductive layer biases the free portion away from the a dielectric layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and each of the second electrically conductive layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer, thereby increasing the capacitance of the capacitor.

7. The capacitor of claim 6, wherein the dielectric layer comprises a first dielectric layer fixed to the first electrically conductive layer and a release layer fixed to the dielectric layer, wherein the anchor portion is fixed to the release layer, wherein the free portion is initially fixed to the release layer, but is released from the release layer to become separated from the underlying dielectric layer.

8. The capacitor of claim 6, wherein the second electrically conductive layers are disposed in rows adjacent to one another.

9. The capacitor of claim 6, wherein the second electrically conductive layers are disposed in columns adjacent to one another.

10. The capacitor of claim 6, wherein the first electrically conductive layer comprises a plurality of electrically conductive layers, one for each second electrically

conductive layer.

11. A capacitor, comprising:

a substrate;

a first electrically conductive layer fixed to the substrate;

a dielectric layer fixed to a portion of the electrically conductive layer; and

a second electrically conductive layer comprising an anchor portion and a free portion, the anchor portion being fixed to the dielectric layer, the free portion being biased away from the dielectric layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and the second electrically conductive layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer, thereby increasing the capacitance of the capacitor.

12. A method for forming a variable capacitor, comprising:

depositing a first layer of an electrically conductive material on a substrate;

depositing a release layer formed of an electrically insulating material on a portion of the first electrically conductive layer;

depositing a second layer of an electrically conductive material on at least a portion of the release layer;

under-cut etching a portion of the release layer under the second layer to release a free portion of the second layer from the release layer, wherein an anchor portion of the second layer remains fixed to the release layer;

wherein the inherent stress profile in the second layer biases the free portion of the patterned second layer away from the release layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and the second layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer.

13. The method of claim 12, further comprising the step of depositing a

dielectric layer between the release layer and the first electrically conductive layer.

14. The method of claim 12, further comprising the step of patterning the second electrically conductive layer into a spring shape prior to the under-cut etch step.

15. The method of claim 12, further comprising the step of patterning the second electrically conductive layer into a plurality of spring shapes.

16. A method of forming a L-C process claim for both combination of capacitors and inductors on same chip allow VCOs.

17 A method of

depositing a first layer of an electrically conductive material on a substrate;

depositing a release layer formed of an electrically insulating material on a portion of the first electrically conductive layer;

depositing a second layer of an electrically conductive material on at least a portion of the release layer;

patterning the second layer into a capacitor plate layer and a microcoil layer;

under-cut etching a portion of the release layer under the second layer to release a free portion of the capacitor plate layer and the microcoil layer from the release layer, wherein an anchor portion of the capacitor plate layer remains fixed to the release layer;

wherein the inherent stress profile in the second layer biases the free portion of the capacitor layer away from the release layer;

wherein, when a bias voltage is applied between the first electrically conductive layer and the second layer, electrostatic forces in the free portion bend the free portion towards the first electrically conductive layer.

wherein the intrinsic stress profile in the microcoil layer biases the free portion of the microcoil layer away from the substrate, forming a loop winding and causing a free end to contact a point on the substrate; and

connecting the free end to the substrate.